CLAIMS

What is claimed is:

1. A logic element, comprising:

a plurality of LUTs (look-up tables);

a plurality of inverters connected to the LUTs;

a plurality of pass gates connected to the LUTs and the inverters;

an output multiplexer connected to the pass gates;

a carry-chain input;

a carry-chain unit connected to the LUTs and the carry-chain input; and

a plurality of controls connected to the LUTs, the pass gates, the output multiplexer, and the carry-chain unit, wherein

in a logic mode the output multiplexer provides a logic function of the controls, and

in an arithmetic mode the output multiplexer provides an arithmetic sum of two logic functions of the controls where the carry-chain unit provides a corresponding carry-chain output.

2. A logic element as claimed in claim 1, wherein

the LUTs include a first LUT, a second LUT, a third LUT, and a fourth LUT,

the inverters include a first inverter that receives input from the first LUT, and a second inverter that receives input from the third LUT, and

the pass gates include a first pass gate that receives input from the first LUT, a second pass gate that receives input from the first inverter, a third pass gate that receives input from the second LUT, a fourth pass gate that receives input from the third LUT, a fifth pass gate that receives input from the second inverter, and a sixth pass gate that receives input from the fourth LUT.

3. A logic element as claimed in claim 1, wherein in the logic mode, the output multiplexer provides a complete function of the controls.

4. A logic element as claimed in claim 1, wherein in the arithmetic mode, the output multiplexer provides an arithmetic sum of two complete functions of a proper subset of the controls.

5. A logic element as claimed in claim 1, wherein at least one control is connected to a plurality of separate controls.

6. A programmable logic device, comprising:

a logic element as claimed in claim 1.

7. A data processing system, comprising:

a programmable logic device as claimed in claim 6.

8. A logic element, comprising:

a plurality of LUTs;

a plurality of data multiplexers connected to the LUTs, the data multiplexers including an output multiplexer;

a plurality of controls connected to the data multiplexers and the LUTs, the controls including an additive control, so that the LUTs, the data multiplexers and the controls define a fracturable LUT having a plurality of fractured outputs, including a first fractured output and a second fractured output;

a carry-chain input; and

a carry-out select multiplexer connected to the carry-chain input, the first fractured output and the second fractured output;

an XOR unit connected to the carry-chain input and the second fractured output, wherein

in a logic mode the output multiplexer provides a first logic function of the controls, and

in an arithmetic mode the XOR unit provides an arithmetic sum of the additive control and a second logic function of the controls where the carry-out select multiplexer provides a corresponding carry-chain output.

9. A logic element as claimed in claim 8, wherein

the multiplexers include an additional output multiplexer, and

in the arithmetic mode the additional output multiplexer provides an additional logic function of the controls.

10. A logic element as claimed in claim 8, wherein in the logic mode, the first logic function provides a complete function of the controls.

11. A logic element as claimed in claim 8, wherein in the arithmetic mode, the second logic function provides a complete logic function of a proper subset of the controls.

12. A logic element as claimed in claim 8, wherein at least one control is connected to a plurality of separate controls.

13. A programmable logic device, comprising:

a logic element as claimed in claim 8.

14. A data processing system, comprising:

a programmable logic device as claimed in claim 13.

15. A logic element, comprising:

a plurality of LUTs;

a plurality of data multiplexers connected to the data multiplexers and the LUTs, the data multiplexers including an output multiplexer;

a plurality of controls connected to the data multiplexers and the LUTs, the controls including an additive control, so that the LUTs, the data multiplexers and the controls define a fracturable LUT having at least one fractured output, including a first fractured output;

a carry-chain input;

a carry-out select multiplexer connected to the carry-chain input, the first fractured output and the additive control; and

an XOR unit connected to the carry-chain input and the first fractured output, wherein

in a logic mode the output multiplexer provides a first logic function of the controls, and

in an arithmetic mode the XOR unit provides an arithmetic sum of the additive control and a second logic function of the controls where the carry-out select multiplexer provides a corresponding carry-chain output.

16. A logic element as claimed in claim 15, wherein

the multiplexers include an additional output multiplexer, and

in the arithmetic mode the additional output multiplexer provides an additional logic function of the controls.

17. A logic element as claimed in claim 15, wherein in the logic mode, the first logic function provides a complete function of the controls.

18. A logic element as claimed in claim 15, wherein in the arithmetic mode, the second logic function provides a complete logic function of a proper subset of the controls.

19. A logic element as claimed in claim 15, wherein at least one control is connected to a plurality of separate controls.

20. A programmable logic device, comprising:

a logic element as claimed in claim 15.

21. A data processing system, comprising:

a programmable logic device as claimed in claim 20.

22. A logic element, comprising:

a plurality of LUTs;

a plurality of data multiplexers connected to the data multiplexers and the LUTs, the data multiplexers including an output multiplexer;

a plurality of controls connected to the data multiplexers and the LUTs, the controls including an additive control, so that the LUTs, the data multiplexers and the controls define a fracturable LUT having at least one fractured output, including a first fractured output;

a carry-chain input;

a carry-out select multiplexer connected to the carry-chain input, the first fractured output and the output multiplexer; and

an XOR unit connected to the carry-chain input and the output mulitplexer, wherein

in a logic mode the output multiplexer provides a first logic function of the controls, and

in an arithmetic mode the XOR unit provides an arithmetic sum of the additive control and a second logic function of the controls where the carry-out select multiplexer provides a corresponding carry-chain output.

23. A logic element as claimed in claim 22, wherein in the arithmetic mode, the output multiplexer receives two complementary inputs.

24. A logic element as claimed in claim 22 wherein in the arithmetic mode, the second logic function provides a complete logic function of a proper subset of the controls.

25. A logic element as claimed in claim 22, wherein in the logic mode, the first logic function provides a complete function of the controls.

26. A logic element as claimed in claim 22, wherein at least one control is connected to a plurality of separate controls.

27. A programmable logic device, comprising:

a logic element as claimed in claim 22.

28. A data processing system, comprising:

a programmable logic device as claimed in claim 27.

29. A logic element, comprising:

a plurality of LUTs;

a plurality of data multiplexers connected to the LUTs, the data multiplexers including an output multiplexer;

a plurality of controls connected to the data multiplexers and the LUTs, the controls including an additive control, so that the LUTs, the data multiplexers and the controls define a fracturable LUT having a plurality of fractured outputs, including a first fractured output and a second fractured output;

a carry-chain input;

a carry-out select multiplexer connected to the carry-chain input and the additive control;

an internal XOR unit connected to the second fractured output, the additive control, and the carry-out select multiplexer; and

an output XOR unit connected to the carry-chain input and the internal XOR unit, wherein

in a logic mode the output multiplexer provides a first logic function of the controls, and

in an arithmetic mode the second fractured output provides a second logic function of the controls, the first fractured output provides a third logic function of the controls, and the output XOR unit provides an arithmetic sum of the additive control and the second logic function of the controls where the carry-out select multiplexer provides a corresponding carry-chain output.

30. A logic element as claimed in claim 29, wherein the internal XOR unit controls the carry-out select multiplexer.

31. A logic element as claimed in claim 29, wherein in the logic mode, the first logic function provides a complete function of the controls.

32. A logic element as claimed in claim 29, wherein in the arithmetic mode, the second logic function and the third logic function each provide a complete logic function of a proper subset of the controls.

33. A logic element as claimed in claim 29, wherein at least one control is connected to a plurality of separate controls.

34. A programmable logic device, comprising:
a logic element as claimed in claim 29.

35. A data processing system, comprising:
a programmable logic device as claimed in claim 34.

36. A logic element, comprising:
a plurality of LUTs;
a plurality of data multiplexers connected to the LUTs, the data multiplexers including an output multiplexer;

a plurality of controls connected to the data multiplexers and the LUTs, the controls including an additive control, so that the LUTs, the data multiplexers and the controls define a fracturable LUT having a plurality of fractured outputs, including a first fractured output and a second fractured output;

a carry-chain input;

a carry-out select multiplexer connected to the carry-chain input and the second fractured output;

an internal XOR unit connected to the second fractured output, the additive control, and the carry-out select multiplexer; and

an output XOR unit connected to the carry-chain input and the internal XOR unit,

wherein

in a logic mode the output multiplexer provides a first logic function of the controls, and

in an arithmetic mode the second fractured output provides a second logic function of the controls, the first fractured output provides a third logic function of the controls, and the output XOR unit provides an arithmetic sum of the additive control and the second logic function of the controls where the carry-out select multiplexer provides a corresponding carry-chain output.

37. A logic element as claimed in claim 36, wherein the internal XOR unit controls the carry-out select multiplexer.

38. A logic element as claimed in claim 36, wherein in the logic mode, the first logic function provides a complete function of the controls.

39. A logic element as claimed in claim 36, wherein in the arithmetic mode, the second logic function and the third logic function each provide a complete logic function of a proper subset of the controls.

40. A logic element as claimed in claim 36, wherein at least one control is connected to a plurality of separate controls.

41. A programmable logic device, comprising:

a logic element as claimed in claim 36.

42. A data processing system, comprising:

a programmable logic device as claimed in claim 41.

43. A logic element, comprising:

a plurality of LUTs;

a plurality of data multiplexers connected to the LUTs, the data multiplexers including an output multiplexer;

a plurality of controls connected to the data multiplexers and the LUTs, so that the LUTs, the data multiplexers and the controls define a fracturable LUT having a plurality of fractured outputs, including a first fractured output, a second fractured output, and a third fractured output;

a carry-chain input; and

an adder unit connected to the first fractured output and the second fractured output and the carry-chain input, wherein

in a logic mode the output multiplexer provides a first logic function of the controls, and

in an arithmetic mode the first fractured output provides a second logic function of the controls, the third fractured output provides a third logic function of the controls, and the adder unit provides an arithmetic sum of the second logic function of the controls and the third logic function of the controls where the adder unit provides a corresponding carry-chain output.

44. A logic element as claimed in claim 43, wherein the adder unit includes a plurality of XOR units.

45. A logic element as claimed in claim 43, wherein in the logic mode, the first logic function provides a complete function of the controls.

46. A logic element as claimed in claim 43, wherein in the arithmetic mode, the second logic function and the third logic function each provide a complete logic function of a proper subset of the controls.

47. A logic element as claimed in claim 43, wherein at least one control is connected to a plurality of separate controls.

48. A programmable logic device, comprising:
a logic element as claimed in claim 43.

49. A data processing system, comprising:
a programmable logic device as claimed in claim 48.

50. A logic element, comprising:
a plurality of LUTs;
a plurality of data multiplexers connected to the LUTs, the data multiplexers including an output multiplexer, a first complementary multiplexer, and a second complementary multiplexer, so that the first complementary multiplexer and the second complementary multiplexer have complementary connections to the LUTs;
a plurality of controls connected to the data multiplexers and the LUTs, the controls including an additive control;
a carry-chain input connected to the output multiplexer; and
a carry-out select multiplexer connected to the carry-chain input, the additive control and the data multiplexers, wherein
in a logic mode the first complementary multiplexer provides a logic function of the controls, and

in an arithmetic mode the output multiplexer provides an arithmetic modification of the logic function of the controls where the additive control is replaced by an arithmetic sum and the carry-out select multiplexer provides a corresponding carry-chain output.

51. A logic element as claimed in claim 50, wherein the arithmetic sum includes the additive control.

52. A logic element as claimed in claim 50, wherein the second complementary multiplexer provides a value of the logic function that is complementary with respect to the additive control.

53. A logic element as claimed in claim 50, wherein the logic function provides a complete function of the controls.

54. A logic element as claimed in claim 50, wherein at least one control is connected to a plurality of separate controls.

55. A programmable logic device, comprising:
a logic element as claimed in claim 50.

56. A data processing system, comprising:
a programmable logic device as claimed in claim 55.